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9. (amended) An integrated circuit device comprising a logic core and a DRAM macro wherein said DRAM macro is a multibank DRAM macro comprising:

(a) a plurality of DRAM memory banks, each bank respectively comprising:

(i) an array of DRAM memory cells,

(ii) bitlines and wordlines, respectively defining columns and rows of the array,

(iii) a dedicated row address decoder circuit,

(iv) a column address decoder circuit ,

(v) dedicated spare rows and columns for redundancy,

(b) a dedicated bank select input for each respective bank, each bank input controlling operation of its respective bank, and

(c) a data path receiver / driver shared by at least two banks.

Remarks

The above amendment is submitted in response to the office action dated October 17, 2002.

The amendment to claims 1 and 9 is supported by Figures 1 and 2 and the discussion in the specification at page 5, lines 22-27, page 6, lines 1-5, and page 7, lines 6-11 and 23-24. Applicants submit that the amendment does not add any new matter to the disclosure.

Applicants will submit a revised Figure 1 upon indication of allowability.

The invention centers on an improved interface for multibank embedded DRAM macro that enables a high performance, easily grown embedded DRAM macro. The macro is characterized by independently accessible banks, each

with a dedicated bank select, as well as dedicated row decoder and dedicated redundancy.

Jun discloses a memory design where a single bank select is shared by two banks, thus, the banks cannot be accessed independently (i.e., simultaneously if desired). Also, Jun does not disclose or suggest the use of a dedicated row decoder for each bank or dedicated redundancy. Thus, applicants submit that the design of Jun is not easily growable.

Dono et al. discloses a DRAM design for a memory chip, not a macro for an embedded DRAM. Dono et al. discloses the use of redundancy in a DRAM device, however, it is not clear that such redundancy is embedded in each bank. Dono et al. does not disclose or suggest the use of a dedicated row decoder for each bank, nor independent bank selects.

Yamaguchi et al. discloses a design where the column access signal is latched to a master flip-flop. It is not apparent that Yamaguchi et al. discloses latching of independent bank selects to a master. Further, Yamaguchi et al. does not disclose or suggest the other aspects of the invention which the combination of Jun and Dono et al. fail to suggest as noted above (i.e., dedicated redundancy in each bank, a dedicated row decoder for each bank, and independent bank selects).

Jeddeloh et al. discloses that many DRAM designs are capable of operating in page mode. Jeddeloh et al. does not disclose or suggest the other aspects of the invention which the combination of Jun and Dono et al. fail to suggest as noted above (i.e., dedicated redundancy in each bank, a dedicated row decoder for each bank, and independent bank selects).

For the above reasons, applicants submit that the claims are allowable over the prior art of record and that the application is now in condition for allowance. Such allowance is earnestly and respectfully solicited.

Respectfully submitted,
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Amendments to the Claims

1. (amended) A multibank DRAM macro, said macro comprising:
   - (a) a plurality of DRAM memory banks, each bank respectively comprising:
     - (i) an array of DRAM memory cells,
     - (ii) bitlines and wordlines, respectively defining columns and rows of the array,
     - (iii) a dedicated row address decoder circuit,
     - (iv) a column address decoder circuit,
     - (v) dedicated spare rows and columns for redundancy,
   - (b) a dedicated bank select input for each respective bank, each bank input controlling operation of its respective bank,
   - (c) a data path receiver / driver shared by at least two banks.

9. (amended) An integrated circuit device comprising a logic core and a DRAM macro wherein said DRAM macro is a multibank DRAM macro comprising:
   - (a) a plurality of DRAM memory banks, each bank respectively comprising:
     - (i) an array of DRAM memory cells,
     - (ii) bitlines and wordlines, respectively defining columns and rows of the array,
     - (iii) a dedicated row address decoder circuit,
     - (iv) a column address decoder circuit ,
     - (v) dedicated spare rows and columns for redundancy,
   - (b) a dedicated bank select input for each respective bank, each bank input controlling operation of its respective bank, and
   - (c) a data path receiver / driver shared by at least two banks.

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